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during synthesis. Logic that is generated from synthesis tools depends highly on the code that is written. A badly formed code would generally create bad logic.

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translated to gates.

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The second half of the book applies Verilog coding to the design of a programmable timer and a programmable logic block for peripheral interface. Topics include comments,



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In this chapter, we discussed of the synthesis-related-features of SystemVerilog which can be used to remove the risk of errors in Verilog. Further, we learn the user-defined types which makes the SystemVerilog codes more readable than the Verilog codes. Also, we learn the 'logic' datatype which can used in place of 'reg' and 'wire'.

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## **10. SystemVerilog for synthesis - FPGA designs with Verilog**

Synthesis Tools Idea: once a behavioral model has been finished why not use it to automatically synthesize a logic implementation in much the same way as a compiler generates executable code from a source program? Synthesis

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programs process the HDL then a.k.a. “silicon compilers” 1 infer logic and state elements

## **Synthesis: Verilog Gates - MIT OpenCourseWare**

Verilog modules that conform to a synthesizable coding style, known as RTL (register-transfer level), can be

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physically realized by synthesis software. Synthesis software algorithmically transforms the (abstract) Verilog source into a netlist , a logically equivalent description consisting only of elementary logic primitives (AND, OR, NOT, flip ...

**Verilog - Wikipedia**



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