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## **Coarse Grain Reconfigurable Architectures Polymorphism**

coarse grain reconfigurable arrays (RAs) with pathwidths greater The KressArray

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is primarily a mesh of rDPUs physically connected through wiring by abutment: no extra routing areas needed.. In 1995 it has been flexibility micro- processor Fig. 2: Bridg-ing the gap. than 1 bit, because fine-grained architectures are much less

## **Coarse Grain Reconfigurable Architectures**

An energy-quality scalable coarse grain reconfigurable architecture (CGRA) based on voltage overscaling (VOS) technique is presented. The approximation level of each Processing Element (PE) in the ...

## **PX-CGRA: Polymorphic approximate coarse-grained ...**

A Coarse-Grained Reconfigurable Architecture for Compute-Intensive MapReduce Acceleration Abstract: Large-scale workloads often show parallelism of different levels. which offers acceleration potential for clusters and parallel processors.

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## **A Coarse-Grained Reconfigurable Architecture for Compute ...**

The coarse grain reconfigurable architectures also have different ways to interconnects processing elements. The connections are multiple bits wide, which implies a higher area usage for a single line. On the other hand, the number of processing elements is typically several orders of magnitude lower than in an FPGA.

## **Survey on Coarse Grained Reconfigurable Architectures**

Assembler level code for coarse grain architectures can be compared to configuration code for FPGAs. In the case of systems comprising a microprocessor / RA symbiosis, only the reconfigurable part is considered for the classification. Programming is done mainly at a kind of assembler level for PADDI-2, MATRIX, and, RAs of REMARC and MorphoSys.

## **Coarse Grain Reconfigurable**

# Get Free Coarse Grain Reconfigurable Architectures Polymorphism In Silicon Cores **Architectures**

Coarse grained reconfigurable array (CGRA) architectures , , , , have been proposed for accelerating computation intensive parts of algorithms residing in several scientific domains. The large number of processing elements (PEs) organized in a 2-dimensional (2D) array and connected with a configurable interconnection network can be used to exploit the applications' inherent parallelism.

## **Resource aware mapping on coarse grained reconfigurable ...**

Reconfigurable architectures become more popular now general purpose compute performance does not increase as rapidly as before. Field programmable gate arrays are slowly moving into the direction of Coarse Grain Reconfigurable Architectures (CGRA) by adding DSP and other coarse grained IP blocks, general purpose processors become more heterogeneous and include sub-word parallelism and even ...

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## **Coarse grained reconfigurable architectures in the past 25 ...**

CCCP: Coarse-Grained Reconfigurable Architecture. CGRAs consist of an array of a large number of function units (FUs) interconnected by a mesh style network. Register files are distributed throughout the CGRAs to hold temporary values and are accessible only by a subset of FUs. The FUs can execute common word-level operations, including addition, subtraction, and multiplication.

## **CCCP: Coarse-Grained Reconfigurable Architecture**

Abstract: Coarse-grained reconfigurable architectures have become increasingly important in recent years. Automatic design or compiling tools are essential to their success. In this paper, we present a retargetable compiler for a family of coarse-grained reconfigurable architectures. Several key issues are addressed.

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## **DRESC: a retargetable compiler for coarse-grained ...**

We introduce Plasticine, a new spatially reconfigurable accelerator architecture optimized for efficient execution of parallel patterns. Plasticine is a two dimensional array of two kinds of coarse-grained reconfigurable units: Pattern Compute Units (PCUs) and Pattern Memory Units (PMUs). Each PCU consists of a reconfigurable

## **Plasticine: A Reconfigurable Architecture For Parallel ...**

Coarse-grained reconfigurable architectures have become increasingly important in recent years. Automatic design or compilation tools are essential to their success. A modulo scheduling algorithm...

## **(PDF) Exploiting loop-level parallelism on coarse-grained ...**

Coarse Grain Reconfigurable Architectures, a Survey

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## **(PDF) Coarse Grain Reconfigurable Architectures, a Survey ...**

Coarse-grained reconfigurable architectures (CGRAs) have the potential to offer performance approaching an ASIC with the flexibility, within an application domain, similar to a digital signal processor. In the past, coarse-grained reconfigurable architectures have been encumbered by challenging programming models that are ei-

## **Designing a Coarse-grained Reconfigurable Architecture for ...**

Title: Coarse Grain Reconfigurable Architectures 1 Coarse Grain Reconfigurable Architectures 2 Announcements. Group meetings this week (sign up sheet) Starting October 8th PSYCH304, 330-6pm ; Today Coarse Grain Architectures ; 3 Motivation for coarse grained architectures. Definition ; FPGA with granularity greater than 1 bit.

## **PPT - Coarse Grain Reconfigurable Architectures PowerPoint ...**



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Hardware Polymorphism – Start with high performance homogeneous substrate – Add coarse-grained reconfigurability to micro-architectural elements – Manage different elements appropriately for different applications

VEC	DSP	UNI	THR	UNI	UNI	UNI	UNI	VEC
UNI	THR	DSP	UNI	UNI	DSP	THR	UNI	UNI
UNI	UNI	4	8/31/05					

## **Polymorphous TRIPS Architecture Exploiting ILP, TLP, and ...**

The coarse-grained reconfigurable architecture ADRES (Architecture for Dynamically Reconfigurable Embedded Systems) and its compiler offer a tool flow to design sparsely interconnected 2D array processors with an arbitrary number of functional units, register files and interconnection topologies.

## **Architectural Exploration of the ADRES Coarse-Grained ...**

This problem can be solved by having a coarse grain array (reconfigurable datapath array, rDPA) and a FPGA on the

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same chip. Coarse-grained architectures (rDPA) are intended for the implementation for algorithms needing word-width data paths (rDPU).

## **Reconfigurable computing - Wikipedia**

Coarse-grained reconfigurable architectures in the past 25 years: Overview and classification. In Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS'16). 235--244. Google Scholar; H. Amano. 2006. A survey on dynamically reconfigurable processors. IEICE Trans Commun. 89, 12 ...

## **A Survey of Coarse-Grained Reconfigurable Architecture and ...**

supporting the development of hybrid architectures such as globally asynchronous, locally synchronous. 1. Introduction In many ways the discussion of "coarse-grained" versus

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“fine-grained” architectures for reconfigurable computing is reminiscent of the early CISC vs. RISC debate. This latter debate was largely about how a

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